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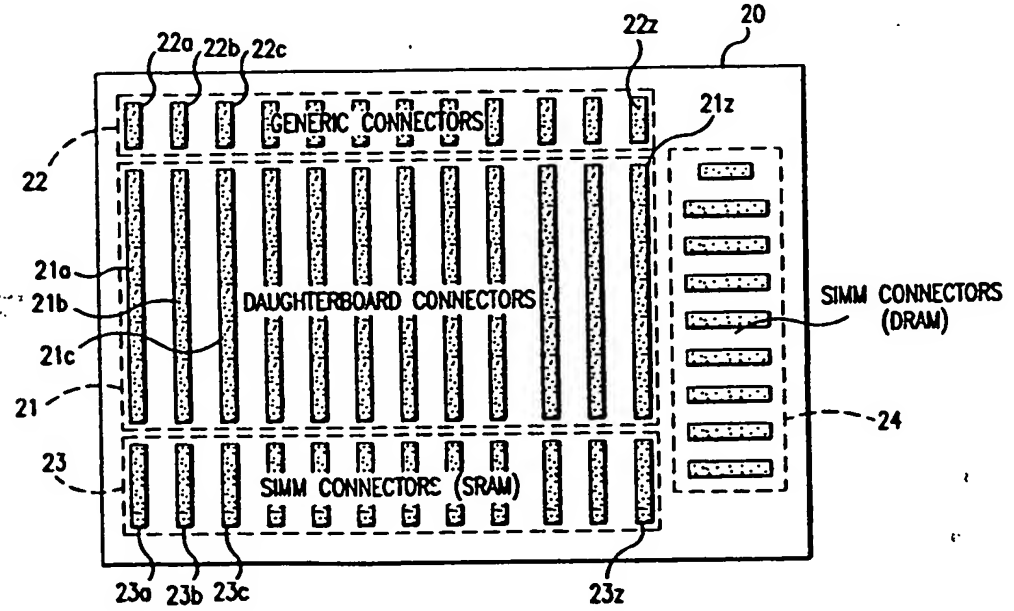

(57) Abstract

A modular computer includes a backplane (20) on which various modules can be interchangeably installed, thereby providing interconnections between the modules. Modules are selected to meet application requirements, and may include, for example, reconfigurable-logic modules (51a-51c) and processor modules (40). The backplane provides connections to extend an effective array (21) of reconfigurable-logic cells across multiple reconfigurable-logic modules without substantial performance limitations. Other connections in the backplane facilitate flexible, high speed I/O (22), while still others distribute programming signals to the various reconfigurable-logic devices in the modular computer (23). The computer can be configured to run both ordinary microprocessor software and highly parallel custom software.

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A MODULAR COMPUTER BASED ON RECONFIGURABLE LOGIC

FIELD OF THE INVENTION:

The present invention relates generally to the field of computer hardware design. In particular, it relates to a modular computer system which can be flexibly arranged into numerous configurations so as to provide both high performance and adaptability to multiple application requirements.

BACKGROUND OF THE INVENTION:

Conventional computer hardware is typically organized into a modular structure which includes a backplane (or motherboard) and various boards (or daughterboards). In such organizations, the backplane serves as a base unit and contains numerous connectors to which boards can be affixed. The boards contain various logical components of the computer hardware, such as microprocessors, memory, I/O circuits, reconfigurable-logic devices, etc. Each board contains an identical set of pins on an edge connector which mounts in one of the backplane connectors. Installing a particular board at a given connector allows the board's pins to electrically contact the backplane through the connector.

The conventional backplane, in addition to providing connectors for affixing boards, includes a bus which electrically connects the pins of boards installed at the various connectors. The bus can be viewed as a collection of parallel wires, each of which connects a particular pin from each of the backplane connectors; a single bus connects all the boards installed at the different connectors. Conventionally, the bus represents the primary means

by which electrical connections between hardware components on different boards ar established.

While this conventional modular computer arrangement allows for great flexibility in terms of hardware configurations, the use of a single bus to interconnect all boards is inherently performance limiting. The bus is, in effect, a single communication resource shared among the various boards. While two boards are using the bus to communicate, any other set of boards needing to communicate must wait until those presently using the bus are finished and have "released" the bus. This type of performance bottleneck is known as bus congestion or contention. Such bus congestion is frequently a fundamental limitation in the I/O bandwidth, memory bandwidth and overall system performance of conventional bus-oriented modular computer designs.

For the past several years, field-programmable gate arrays (FPGAs) have been the fastest growing segment of the semiconductor market. FPGAs are reconfigurable-logic circuits in which the connections between various logical components are electrically programmable. Typically, an FPGA is organized as a regular array of identical cells, each of which contains one or more combinational or sequential logic circuits. In most commercially available FPGAs, the individual cells include some type of storage register and a number of combinational gates. Besides the cells, an FPGA also includes programmable connection resources between various (primarily neighboring) cells in the array. An FPGA is configured by electronically selecting both the configurations of individual cells so as to determine the logical operation performed by each cell and the configuration

of the inter-cell connection resources so as to determine the logical connections between cells. Commercially available FPGAs can be electronically configured or reconfigured within milliseconds to implement a vast range of logical circuits.

Researchers have recognized that FPGAs can be used to achieve dramatic increases in computer performance. See, for example, P. Bertin, D. Roncin and J. Vuillemin, "Programmable Active Memories: a Performance Assessment", First International ACM/SIGDA Workshop on Field Programmable Gate Arrays, February 14, 1991 (additional material distributed at conference). A programmable active memory (PAM) is a hardware co-processor consisting of several FPGAs and some local memory organized onto a single board and interfaced to a host processor using a standard bus-oriented interface. As reported, PAMs have been used to achieve dramatic speedup for a variety of compute-intensive applications.

Other PAM-like add-on board approaches have been reported. The article "Building and Using a Highly Parallel Programmable Logic Array" by M. Gokhale, W. Holmes, A. Kosper, S. Lucas, R. Minnich, D. Sweely and D. Lopresti, IEEE Computer, January, 1991, reports a speedup of 330 over a Cray-2 supercomputer on a pattern matching problem using two PAM-like add-on boards in a Sun workstation. The article notes, nevertheless, that the add-on boards (collectively termed "Splash") are I/O-limited and that many applications could run an order of magnitude faster with better I/O. Another add-on board approach is reported in the article "The Use of FPGAs in a Novel Computing Subsystem" by I. Buchanan and T. Kean, First International ACM/SIGDA Workshop on Field Programmable Gate Arrays, February 14, 1991.

Generally speaking, one key to achieving extremely high computational throughput using a PAM or other similar reconfigurable-logic add-on board lies in the ability to perform parallel data operations along an entire dimension of an array of cells. Once data is loaded into the array, processing can proceed at very high speed. In fact, the processing speed of a PAM-type reconfigurable-logic board, as previously noted, may quickly exhaust the I/O bandwidth of the bus attaching the board to the host processor. Moreover, one may wish to install multiple PAM-type reconfigurable logic boards so as to expand the effective size of the reconfigurable logic array. Unfortunately, installing multiple reconfigurable logic boards on a conventional computer bus does not achieve the desired result. The bus, as a shared resource, fails to provide adequate bandwidth and availability to support the communication between sections of an extended reconfigurable logic array. Thus, there remains a present need for a modular computer system which provides for modular expandability without imposing performance limiting I/O restraints on the reconfigurable logic.

SUMMARY OF THE INVENTION:

Accordingly, one object of the present invention is an improved modular computer including both an expandable reconfigurable-logic section and a conventional microprocessor.

Another object of the invention is an improved modular computer including both reconfigurable logic and a conventional microprocessor wherein the reconfigurable logic can be configured to allow the microprocessor to run conventional software.

Still another object of the present invention is an improved modular computer based on reconfigurable logic wherein a plurality of reconfigurable-logic modules can be installed to provide an expanded reconfigurable-logic array.

Still another object of the invention is an improved modular computer including reconfigurable logic wherein flexible I/O terminals in each reconfigurable-logic module allow full speed parallel I/O into either dimension of an expanded reconfigurable-logic array.

Still another object of the invention is an improved modular computer based on reconfigurable logic wherein multiple reconfigurable-logic modules can be installed to form a cylindrically connected array.

Still another object of the invention is to replace a conventional bus with an array of configurable-logic elements that provide for multiple simultaneous communication paths between various system elements.

In accordance with the invention, an improved modular computer includes a backplane having a plurality of receptacles at which modules may be installed. At any given time, each receptacle accommodates one of a plurality of different modules, including a processor module, a reconfigurable-logic module or other module. Connections between receptacles in the backplane are organized such that reconfigurable-logic modules installed at adjacent receptacles are directly connected so as to form an expanded reconfigurable-logic array. The backplane further provides for distribution of various control and configuration signals to all installed modules.

Any number of reconfigurable-logic modules, limited by the number of receptacles, can be installed at the receptacles to meet system requirements. Each reconfigurable-logic module includes one or more FPGAs connected such that an effective overall two-dimensional array of cells is formed. Connectors on each reconfigurable-logic module provide for I/O from cells on the boundary of the two-dimensional reconfigurable-logic array. Certain connectors are used to expand the size of the array in one dimension while others are advantageously used to interface with a local memory and other generic I/O devices.

The backplane may also provide receptacles for memory modules. Within the modular computer, memory takes two forms. Static random-access memory (SRAM) is used to implement local memories associated with the processor, reconfigurable-logic or other boards. A dynamic random-access memory (DRAM) associated with a processor module allows for execution of conventional microprocessor software.

The processor module includes a conventional microprocessor advantageously interfaced through one or more FPGAs. The FPGA is configured so as to emulate the expected interface between the microprocessor and the DRAM and/or other I/O devices. An EPROM memory on the processor board provides for power-up configuration of the processor module's FPGA.

Because cells of the FPGA have both programmable connection resources and one or more combinational or sequential logic circuits, the modular computer of the present invention provides both communication and computation capabilities in the single structure of the expandable array of FPGAs. As a result, the present invention eliminates bus congestion while

providing the flexibility and expandability of a modular system.

BRIEF DESCRIPTION OF THE DRAWINGS:

These and other features and advantages of the present invention are illustrated in the following drawings, in which:

Fig. 1 depicts a conventional housing used to encase the modular computer;

Fig. 2 depicts a top view of a motherboard and its various daughterboard connectors;

Fig. 3 depicts the external connections for a daughterboard;

Fig. 4 depicts the components and external connections for a processor board; and

Fig. 5 depicts a preferred organization of components in a reconfigurable-logic board.

DETAILED DESCRIPTION OF THE INVENTION:

Referring now to Fig. 1, a conventional housing 10 encases the preferred embodiment of the improved modular computer. The front panel 11 of housing 10 may include an aperture 13 for inserting and removable magnetic or other disk cartridges. Similarly, the back panel 12 may include a plurality of back panel connectors (not shown) which interface with I/O devices such as a keyboard, mouse, display monitor, disk drive, tape drive, printer, etc. Within housing 10 are most of the components typically found in a standard personal computer chassis. These include a power supply, motherboard, and mounting brackets for hard and floppy disk drives.

The previous Summary of the Invention refers to a backplane having receptacles to which modules attach. The text describing the preferred embodiment, below,

refers to a motherboard having daughterboard connectors to which daughterboards attach. These changes in terminology are in no way intended to be limiting; rather, the terms "motherboard" and "daughterboard" have been adopted merely to provide a more concrete and easily understandable description of the physical components in the preferred embodiment.

Referring now to Fig. 2, a motherboard 20 mounts to the interior bottom wall of housing 10. Viewed from the top in Fig. 2, motherboard 20 includes a plurality of daughterboard connectors 21, generic connectors 22, static random access memory (SRAM) single inline memory module (SIMM) connectors 23 and a plurality of dynamic random access memory (DRAM) SIMM connectors 24.

Overall, housing 10 and motherboard 20 are designed to maximize the use of standard parts wherever such use does not substantially limit the performance of the computer. Accordingly, the preferred embodiment of the improved modular computer provides for use of off-the-shelf SIMM memory modules which may be installed at connectors 23 and 24. Similarly, logic components are mounted onto daughterboards which are interchangeably installed at daughterboard connectors 21. In accordance with the invention, however, the structure of the daughterboards and the interconnections between daughterboards provided by motherboard 20 and connectors 21, 22, 23, and 24, are organized in a novel manner such that extremely high performance can be realized using reconfigurable logic. This modular organization also advantageously provides the ability to run standard microprocessor software. These aspects and advantages of the invention will become

apparent from the discussion of the processor board and the reconfigurable-logic board in Figs. 3-5 below.

Still referring to Fig. 2, each of the daughterboard connectors 21a-z is a multi-pin connector. Some of these pins are connected in a bus and commonly connected among all the daughterboards while others connect only to adjacent daughterboards and still others connect to particular generic connectors 22 or SRAM SIMM connectors 23. For example, daughterboard connector 21b has certain pins connecting to a bus shared by all other daughterboards, other pins connecting only to adjacent daughterboard connector 21a, still other pins connecting only to adjacent daughterboard connector 21c, still other pins connecting to respective generic connector 22b and still other pins connecting to respective SRAM SIMM connector 23b.

Reference is now made to Fig. 3 which depicts the electrical connections to and from a daughterboard 30 via the daughterboard connectors 21. Each daughterboard 30 electrically contacts its daughterboard connector with the following sets of terminals: (1) control terminals 34; (2) left I/O 35L and right I/O 35R terminals; (3) front I/O terminals 36; and (4) rear I/O terminals 37. Of course, each daughterboard connector 21, SRAM SIMM connector 23 and DRAM SIMM connector 24 also includes power and ground terminals which are assumed but not depicted in the drawings. Control terminals 34 provide for distribution of clock and reset signals as well as signals for configuring the reconfigurable logic. The function of particular control signals 34a-h will be discussed in connection with the programming of reconfigurable-logic board 50 (Fig. 5). The primary data connection between daughterboards occurs via the

left and right I/O terminals 35L and 35R respectively. Motherboard 20 provides for electrical connection between the left I/O terminals 35L of a given daughterboard 30 and the right I/O terminals 35R of one of the daughterboards installed at an adjacent daughterboard connector 21 and for electrical connection between the right I/O terminals 35R of the given daughterboard and the left I/O terminals 35L of the daughterboard installed at the other adjacent daughterboard connector 21. At the ends, the left and right I/O signals wrap around, as do the configuration signals.

For example, the daughterboard installed at connector 21b has its left I/O terminals 35L connected to the right I/O terminals 35R of the daughterboard installed at connector 21a. Further, the right I/O terminals 35R of the daughterboard at connector 21b connects to the left I/O terminals 35L of the daughterboard at connector 21c. The wrapping around of the left and right I/O terminals occurs between daughterboard connectors 21a and 21z. Motherboard 20 connects the left I/O terminals 35L of the daughterboard installed at connector 21a to the right I/O terminals 35R of the daughterboard at connector 21z.

The connections provided between adjacent daughterboards via the left and right I/O terminals 35L and 35R can be viewed, in a sense, as an improved data bus. In fact, reconfigurable-logic circuits on the daughterboards may be configured to connect the left and right I/O terminals (of each board) so as to form a virtual data bus. Advantageously, however, not having to rely on a conventional data bus connecting daughterboard connectors 21a-z eliminates bus contention problems and leads to substantial

performance improvement. The reconfigurable logic can operate at its full potential, without the choking effect of bus contention associated with other add-on reconfigurable-logic board approaches.

Motherboard 20 connects the front I/O terminals 36 of each daughterboard 30 to its respective SRAM SIMM connector. Thus, associated with each daughterboard 30 is an optional local memory installed at the SRAM SIMM connector 23.

Mother board 20 also provides connections between the rear I/O terminals 37 of a daughterboard 30 and the respective generic connector 22. The generic connector 22 provides considerable flexibility in configuring the improved modular computer for particular application needs. For example, several of the generic connectors 22 may be linked using a ribbon cable or other connection means to form a common bus. Generic connectors 22 may also be used to connect with various back panel 12 connectors which interface to external devices. Further, the generic connectors may be used to connect with various components within housing 10, such as DRAM 24 or hard/floppy disks (not shown).

One important application of the I/O access provided to each daughterboard 30 via generic connectors 22 is high speed parallel I/O, such as the so-called "disk striping" or redundant arrays of inexpensive disks (RAID) techniques. See, for example, P. Chen, *An Evaluation of Redundant Arrays of Inexpensive Disks Using an Amdahl 5890,"* M.S. thesis, Computer Science Division, Tech Report UCB/CSD 89/056, 1989; M.Y. Kim, *Synchronized Disk Interleaving*, IEEE Transactions on Computers C-35:11, November, 1986; K. Salem and H. Garcia-Molina, *Disk Striping*, IEEE 1986 International Conference on Data Engineering, 1986.

These approaches involve partitioning a single file into K similarly sized pieces and storing each piece on one of K disk drives. The present invention permits each disk drive to be independently controlled through a different generic connector 22 interfaced to a reconfigurable-logic board 50. Thus, the modular architecture of the invention can easily be configured to control arrays of multiple disks and is ideally suited to such high-bandwidth parallel I/O applications.

Reference is now made to Fig. 4 which depicts the processor board 40 and the various connections therefrom and thereto. Processor board 40 is installed at one of the daughterboard connectors 21 and serves two primary functions in the modular computer. First, it provides one means of supervising, synchronizing and controlling the configuration of the various reconfigurable-logic devices within the modular computer system. Second, it provides a means by which the modular computer can be configured and adapted to run ordinary software, thus providing an important compatibility feature.

Processor board 40 includes three main components: a microprocessor 41, an FPGA 42, and a non-volatile memory 43. Memory 43 may be used to configure FPGA 42 at power-up. FPGA 42 implements a flexible interface between processor 41 and numerous other components within the modular computer. In particular, FPGA 42 is configured to interface between the data 45 and address 46 busses of microprocessor 41 and the control signals 34 which are distributed to the daughterboard connectors 21 by motherboard 20. FPGA 42 optionally provides interfaces from microprocessor 41 to such destinations as non-volatile memory 43, various motherboard pins 47a, various back

panel connectors 47b, DRAM 47c, SRAM and other devices 47d such as hard and floppy disk drives. The method by which control signals 34 are disseminated from processor board 40 to the various destination FPGAs will be discussed later in connection with the reconfigurable-logic boards 50 (Fig. 5).

Fig. 4 depicts various sources from which such configuration information might be derived. For example, processor 41 may utilize prestored configurations in memory 43 to generate appropriate control signals 34. Alternatively, processor 41 could extract configuration information from DRAM 47c, SRAM or other secondary storage 47d and similarly generate appropriate configuration signals 34 for further distribution. It should also be noted that, if no processor board 40 is installed in the motherboard 20, configuration of various FPGAs can still be accomplished via a back panel connector interfaced to provide the control signals 34.

Non-volatile memory 43 includes the necessary code to configure FPGA 42 to provide the expected interface for processor 41, thereby allowing processor 41 to execute ordinary software. This involves configuring FPGA 42 such that it reacts appropriately to bus control signals 44 and provides the necessary connections from the address and/or data busses 45 and 46 to the DRAM 47C and other I/O devices 47D. Use of an FPGA to provide a flexible interface between a microprocessor and other computer system resources such as memory and I/O devices is known in the art of conventional computer design. However, such use is typically aimed at providing plug-in compatibility of future microprocessors which may require slight changes in the interface, bus protocol, or timing requirements. The present invention, in contrast,

finds processor 41 placed in a radically different environment; FPGA 42 advantageously emulates an ordinary interface 44-46 to processor 41, thereby endowing processor 41 with the capability to execute conventional software in the modular computer environment.

Reference is now made to Fig. 5 which depicts a reconfigurable-logic board 50 illustratively comprises four FPGAs 51a-d. Each FPGA comprises a square array of identical cells and provides I/O terminals at its front, rear, left and right boundaries. Within reconfigurable-logic board 50, certain I/O terminals 52 of FPGAs 51a-d are linked front-to-rear so as to form an expanded array in the front-to-rear dimension, as depicted in Fig. 5.

The array of cells on reconfigurable-logic board 50 can, if necessary, be further extended in the front-to-rear dimension using the rear I/O terminals 37 and linking through a generic connector 22 to another reconfigurable-logic board 50.

In the left-to-right dimension, motherboard 20 provides for left-to-right linking of I/O terminals 35L and 35R so as to expand the array. Since the right and left I/O terminals at either ends of the set of daughter board connectors 21 are linked, the cells of multiple reconfigurable-logic boards 50 installed at daughterboard connectors 21 effectively form a cylindrical array geometry. Thus, through the various provisions for expandability including the left-to-right I/O connections between daughterboards, the generic connectors and the cylindrical closing of the array in the left-to-right dimension, a very large number of reconfigurable-logic cells can be linked to form an effectively contiguous array which does not

suffer from the conventional I/O or bus contention bottlenecks.

As depicted in both Figs. 3 and 5, each daughterboard connects to four sets of control signals 34. One set of control signals 34 is provided to each FPGA 51a-d on reconfigurable-logic board 50. Each of the sets of control signals 34 is used to configure an FPGA at a particular location, such as 51d, on all reconfigurable-logic boards 50. The preferred embodiment of reconfigurable-logic board 50 employs CLi6000 Series Field-Programmable Gate Arrays, as described in the Product Literature, Rev. 1B, Concurrent Logic, Inc., May 1992, incorporated herein by reference. Figs. 3 and 5 depict the individual control signals 34, four of which 34a-d are bussed and common among all daughterboard connectors 21a-z and another four of which 34e-h connect only between adjacent daughterboard connectors. Among the commonly bussed signals, Clock 34a and Reset 34b control the clock and reset functions of flip-flops within the individual cells of the FPGAs. The REBOOT line 34c is used to assert a request for a system-wide restart, and CON(low) 34d indicates, when asserted low, that the configuration process is in progress.

Actual configuration data is distributed via the adjacently connected terminals 34e-h. Configuration signals DO 34e and CCLK 34g originate from processor board 40 or a back-panel connector and cascade from one reconfigurable-logic board 50 to the next in order to configure all FPGAs 51 as required. The cascading of configuration signals occurs via motherboard 20 which provides connections between the DATAOUT 34f and CLKOUT 34h terminals of a given board and terminals 34e and 34g of the daughterboard 30 installed at the left-adjacent daughterboard connector 21. Thus, for

each FPGA 51a-d on a reconfigurable-logic board 50, each FPGA receives configuration signals 34e and g which either contain configuration data for the given FPGA or configuration data for some similarly positioned FPGA on another board 50. Configuration data D0 is received by each FPGA 51a-d and read in using CCLK 34g. Each FPGA appropriately decodes header information in its D0 signal to determine whether or not to pass this information to another FPGA. Depending on the header, each FPGA 51a-d may relay (or cascade) the configuration data to its left-adjacent neighbor board via its DATAOUT terminal 34f which it clocks using the CLKOUT terminal 34h. Each FPGA receiving the cascaded configuration data makes a similar determination (based on the header) and utilizes or relays the signals accordingly. Advantageously, headers provide the ability to selectively reconfigure only a portion of the FPGAs on one or more reconfigurable-logic boards 50, thus saving reconfiguration time and minimizing disruption to ongoing computations in other portions of the FPGAs.

Generally speaking, the cylindrical closing of the connections between adjacent daughterboards (i.e., daughterboard connectors 21a and 21z are considered adjacent) allows for flexibility in the positions at which various boards may be installed. Boards, other than reconfigurable-logic boards 50, that do not make use of the left and right I/O terminals 35L and R and/or the configuration terminals 34 may simply route these signals through the daughterboard connector 21 to maintain signal continuity. Each empty daughterboard connector 21 may require the installation of a dummy board in order to maintain the same signal continuity.

Although the description of the preferred embodiment has focused on only two types of boards which form the core of a simple but powerful modular computer, numerous other modules and/or alterations in the design of the modular computer could be included to meet specific application requirements. For example, daughterboards might contain one or more digital signal processors, floating point or other mathematical coprocessors, RAM and/or neural network devices or cells. The previously described modular computer can be configured into either an attached computing unit, containing largely reconfigurable-logic boards and SRAM and communicating via back-panel connectors, or a complete computer system, including a processor board, reconfigurable-logic boards, SRAM, DRAM, hard and floppy disks, optional video and/or analog boards, etc. Configurations of the modular computer can be used to accelerate such applications as file servers, database processing, image processing, multi-media computing, network protocol processing, and real-time data acquisition. Such applications may require inclusion of additional boards 30 containing other digital or analog circuits not previously described herein. Such additional boards, to the extent that they adhere to the modular organization and interface framework described herein, shall be considered within the scope of the present invention.

Additional features and/or flexibility could also be added to the motherboard. For example, the motherboard could be expanded to accommodate multiple parallel rows of daughterboards and/or the modular computer might contain multiple motherboards. Some of the electrical connections provided by the motherboard could be made configurable. Alternatively, certain

configurable connections, for example those between the DRAM and the daughterboards, could be hard-wired into the motherboard, thus potentially providing higher performance.

Different array topologies for the reconfigurable-logic section, such as spiral, toroidal, or hypercube, are practically realizable using the modular organization described herein. Also, the connections between modules need not be electronic; any technique capable of transmitting logical signals, such as optical coupling, will suffice to realize the advantages of the invention. Finally, it is also possible to eliminate the need for a backplane (or motherboard) entirely. This is accomplished by forming modules which provide the necessary connections by abutment (e.g., the modules plug together one above another to form a vertical stack).

Having described a novel modular organization for computer components and an exemplary configuration, including a processor and reconfigurable-logic board, based on the organizational framework, numerous alternatives, extensions and improvements will be apparent to those skilled in the art. Accordingly, the present invention shall be defined only in accordance with the following claims and equivalents thereto.

WHAT IS CLAIMED IS:

1. A modular computer comprising:

a plurality of modules each including reconfigurable-logic circuits, first electrical terminals and second electrical terminals; and

module connection means including a plurality of installation ports for interchangeably installing modules thereat, said module connection means providing connections between the electrical terminals of said modules whereby if a particular module is installed at a particular port and two other modules are installed at ports adjacent to said particular port then the first terminals of said particular module connect to the second terminals of one of said other modules while the second terminals of said particular module connect to the first terminals of the other of said two other modules.

2. A modular computer as defined in claim 1 wherein said first terminals of said two other modules are not electrically connected to each other and said second terminals of said two other modules are not electrically connected to each other by said module connection means.

3. A modular computer as defined in claim 1 wherein each module further comprises control signal terminals and said module connection means further provides electrical connections between the control signal terminals of modules installed at all installation ports.

4. A modular computer as defined in claim 1 wherein a plurality of said modules are reconfigurable-logic

modules, each reconfigurable-logic module being adapted such that the reconfigurable-logic circuits therein form a two-dimensional array, said array being connectable with the arrays of other reconfigurable-logic modules installed at adjacent installation ports so as to extend the array in one dimension.

5. A modular computer as defined in claim 4 wherein the connections between the arrays of two adjacently installed reconfigurable-logic modules are between the first terminals of one of the modules and the second terminals of the other module.

6. A modular computer as defined in claim 1 wherein each module further includes memory terminals for connecting said module to a storage means associated therewith.

7. A modular computer as defined in claim 1 wherein each module further includes generic terminals for connecting said module to I/O or memory resources in said computer.

8. A modular computer comprising:

a processor module including a microprocessor;

a plurality of reconfigurable-logic modules, each including reconfigurable-logic cells connected to form an array; and,

a module connecting means for connecting said processor module and said reconfigurable-logic modules such that said reconfigurable-logic modules form an extended array of reconfigurable-logic cells and said processor module can realize

connections between said microprocessor and said extended array.

9. A modular computer as defined in claim 8 further comprising a dynamic memory connected to said processor module.

10. A modular computer as defined in claim 9 wherein said processor module further comprises a reconfigurable-logic devices, said reconfigurable-logic device in the processor module being configurable to provide an interface between the microprocessor and the dynamic memory module so as to allow the microprocessor to run ordinary software.

11. A modular computer as defined in claim 8, wherein said module connection means further comprises a plurality of module receptacles whereat processor and/or reconfigurable-logic modules can be interchangeably installed.

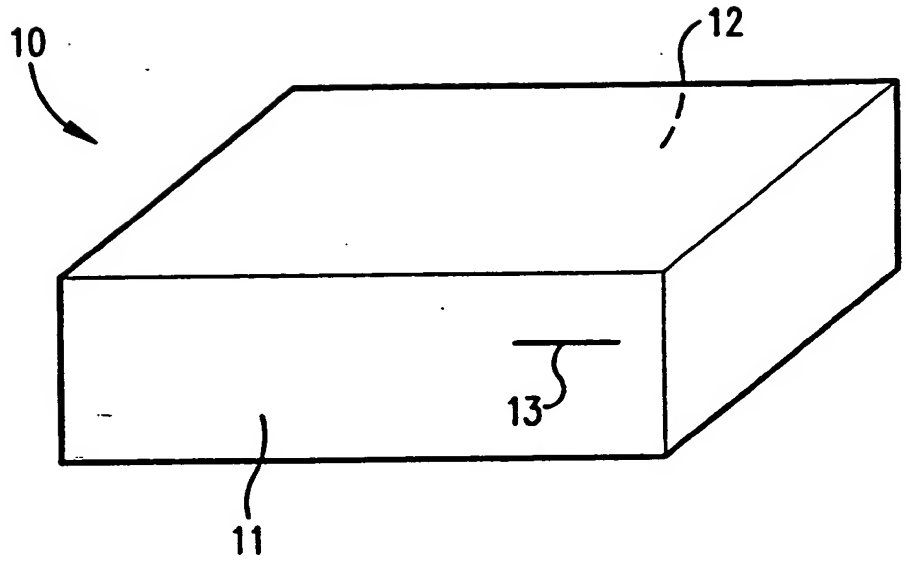

FIG. 1

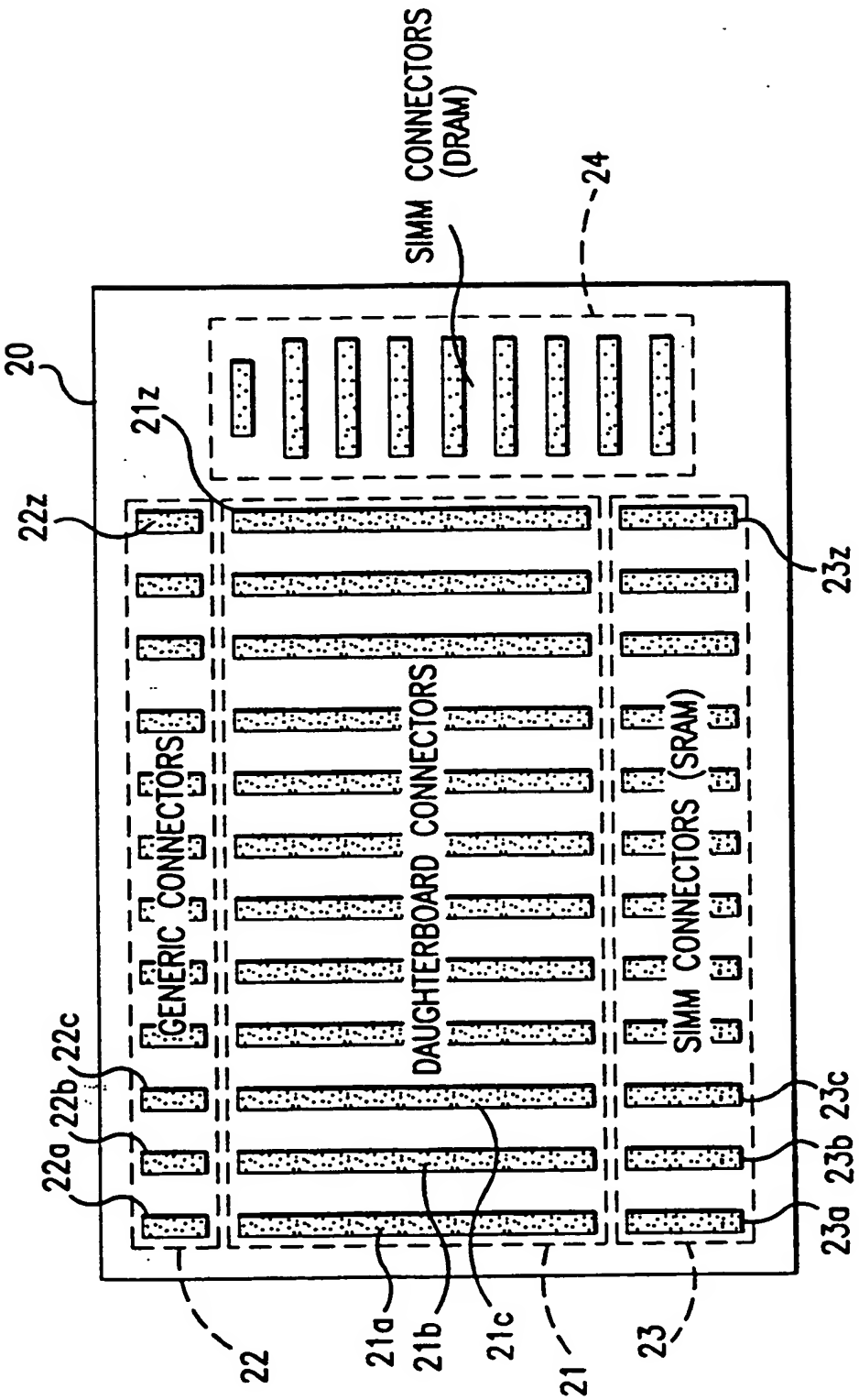
SIMM CONNECTORS (DRAM)
24
20
21z
22z
23z
GENERIC CONNECTORS
DAUGHTERBOARD CONNECTORS
SIMM CONNECTORS (SRAM)
22c
22b
22a
23c
23b
23a
22
21a
21b
21c
21
23

FIG.2

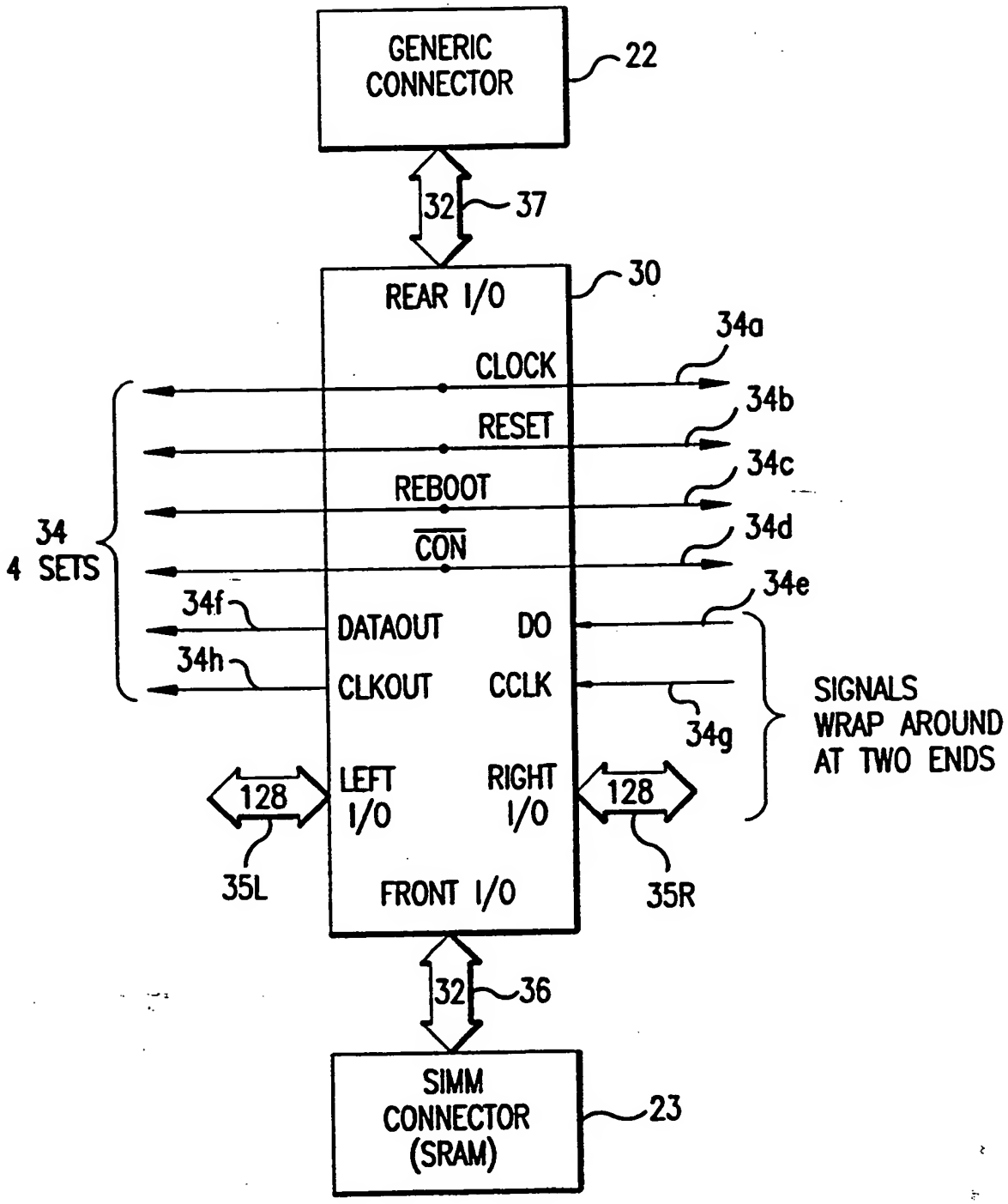
GENERIC CONNECTOR
22
32
37
REAR I/O
30
34a
CLOCK
34b
RESET
34c
REBOOT
34d
CON
34e
34
4 SETS
34f
DATAOUT
DO
34h
CLKOUT
CCLK
34g
SIGNALS WRAP AROUND AT TWO ENDS
128
LEFT I/O
RIGHT I/O
128
35L
FRONT I/O
35R
32
36
SIMM CONNECTOR (SRAM)
23

FIG.3

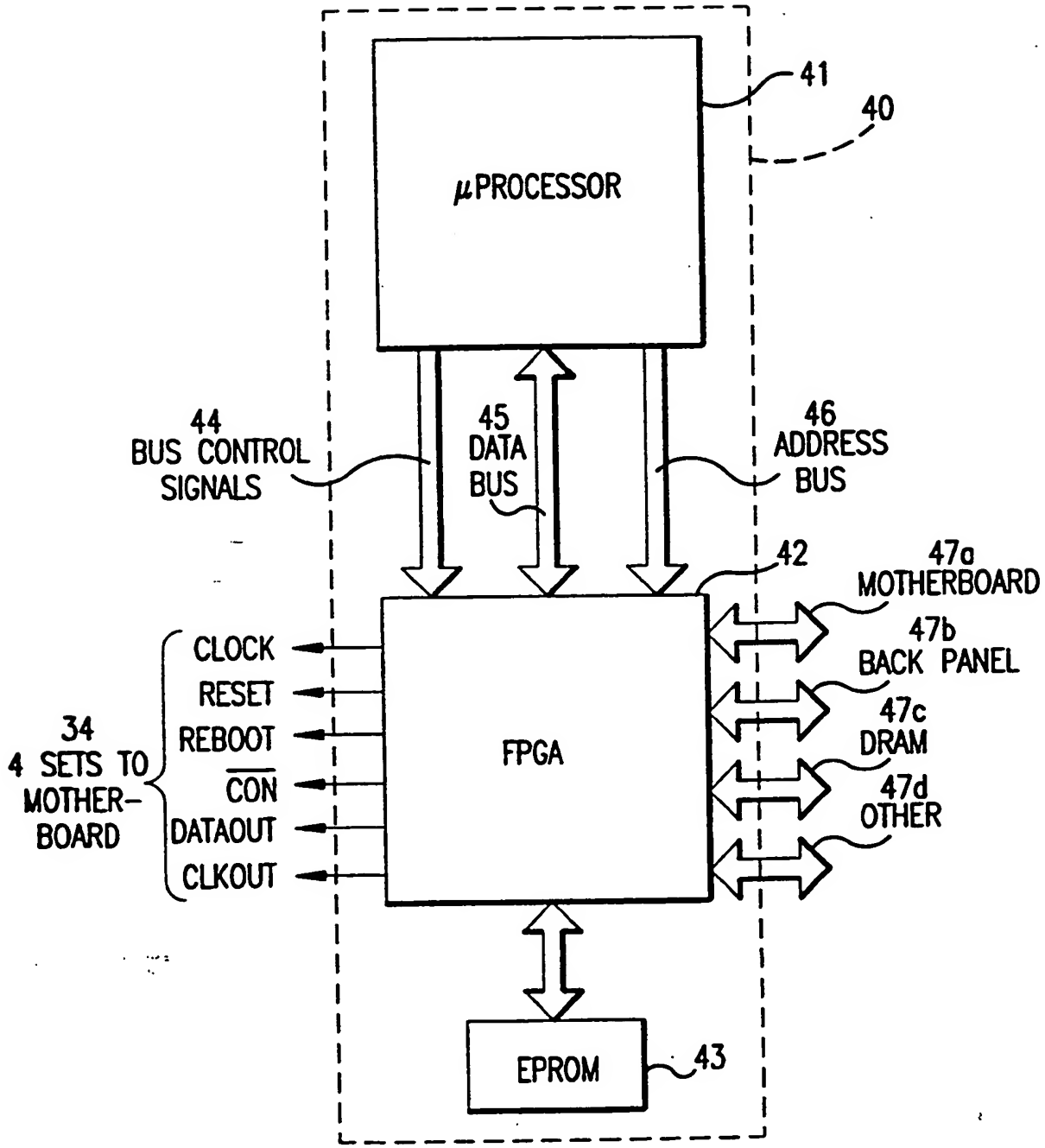
41
40
μPROCESSOR
44
BUS CONTROL
SIGNALS
45
DATA
BUS
46
ADDRESS
BUS
42
47a
MOTHERBOARD
47b
BACK PANEL
47c
DRAM
47d
OTHER
34
4 SETS TO
MOTHER-
BOARD
CLOCK
RESET
REBOOT
CON
DATAOUT
CLKOUT
FPGA
EPROM
43

FIG.4

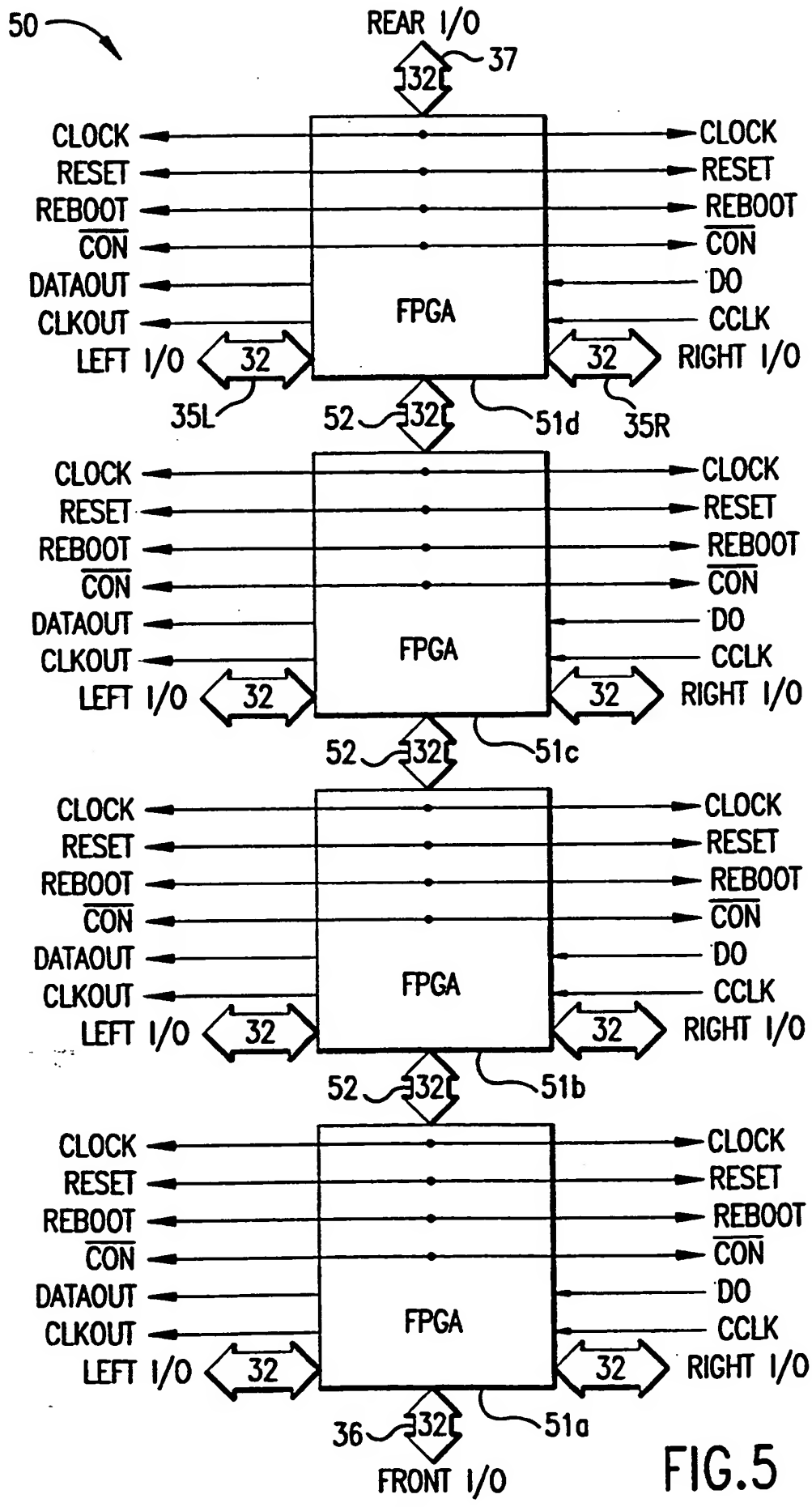
50
REAR I/O
37
32
CLOCK
RESET
REBOOT
CON
DATAOUT
CLKOUT
LEFT I/O
32
FPGA
CLOCK
RESET
REBOOT
CON
DO
CCLK
32
RIGHT I/O
35L
52
32
51d
35R
51c
51b
36
FRONT I/O
51a

FIG.5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/05557

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : G06F 15/00
US CL : 395/800,375,500
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/800,375,500

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched.

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS,INSPEC
search terms: FGPA,PAM,modular computer, ASIC,reconfigurable, board

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A 4,635,192 (Ceccon et al) 06 January 1987, abstract,figures 1,13 ,col. 3-4	1-3
A	US, A 4,856,091 (Taska) 08 August 1989 ,figure 1,col. 2	1
X ---- Y	US, A 4,933,838 (Elrod) 12 June 1990, figure 3,abstract,col. 2	1-3 -------- 7,8,11
Y	US, A 4,777,615 (Potash) 11 October 1988, col. 3-4,figure 1	7,8
A	US, A 4,922,409 (Schoellkopf et al) 01 May 1990 , abstract	1
X	US,A 4,658,333 (Grimes) 14 April 1987, col. 2, abstract, figure 1	1

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
17 August 1993

Date of mailing of the international search report
12 NOV 1993

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	IEEE Colloquium on ' User-Configurable Logic- Technology and Applications', 1991, Kean , "Configurable array logic technology at chip and board level", pages 3/1-3/3	8-10 ----- 11